Stavan Ruparelliya

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Professional Summary

Embedded Software Engineer with 6+ years of experience in Edge AI, Embedded Linux, and SoC platforms. Transitioning into Design Verification with a strong foundation in Digital Design and Verilog HDL. Skilled in Python, Shell scripting, low-level debugging, and hardware-software integration. Currently building expertise in Verilog, constrained-random verification, and functional coverage.

Tech-Stacks

Technology	VLSI Design, Verification, SoC/ASIC Verification, Semiconductor, Embedded Systems, Artificial Intelligence, Computer Vision, Edge Computing
Concepts	ASIC Design/Verification, CPU Design, Computer Architecture, Digital Logic Design, Functional Verification
Languages	Verilog, C, C++, Python, Shell
Protocols	I^2C, SPI, UART, CAN, USB
Tools	Git, GitHub, GDB, Valgrind, Docker
Operating Systems	Linux, Embedded Linux, Windows

Professional Experience

Sr. AI Research Engineer L1, Dec 2025 – Present
Mantra Smart Identity (Mantra Softech), Ahmedabad, India.

- Designed, developed, and optimized computer vision models and GStreamer-based media pipelines for an Edge AI product, owning the end-to-end model lifecycle — development, training, conversion/optimization, and deployment — to enable real-time video analytics on embedded platforms.
- Conducted market research to analyze competitor products and industry trends, providing insights that guided product strategy and feature development.

Senior Software Engineer, Mar 2025 – Oct 2025
Tata Elxsi Limited, Bangalore, India. **Client :** Comcast Corporation

- Developed AI/ML-based text and image summarization pipelines for multimedia applications on embedded platforms for Comcast, leveraging deep learning models for efficient content understanding and compression.
- Deployed and optimized AI inference pipelines on edge devices within embedded Linux environments, with a focus on performance profiling, debugging, and resource optimization.

Software Engineer, Jul 2021 – Mar 2025
eInfochips (An Arrow Company), Ahmedabad, India.

- Designed and implemented a video analytics solution using C/C++ and Python, integrating deep learning and computer vision models with embedded hardware for real-time edge inference. Led hardware-software co-design efforts, bridging embedded systems with AI pipelines for seamless integration and deployment.
- Applied quantization and pruning techniques to computer vision models, achieving high accuracy with reduced computational overhead. Built a camera simulator with a modular image processing pipeline, facilitating rapid prototyping and client POC validation.
- Collaborated directly with U.S. and European clients, collaborating across engineering, product, and client teams to deliver solutions within agile development cycles.

Project Trainee Engineer Jan 2021 – Jun 2021
eInfochips (An Arrow Company), Ahmedabad, India.

- Completed training in C++, Python, embedded systems, and Linux internals with hands-on system programming and memory management projects.
- Contributed to client deliverables and assisted in building future project PoCs.

Technical Projects

FIFO Design and Verification | **RTL Design** *Verilog; EDA Playground*

- Designed a parameterized synchronous FIFO in Verilog RTL with configurable depth and data width, implementing read/write pointer logic and full/empty flag generation for reliable data buffering between clock-synchronous interfaces.
- The simulated design was validated on EDA Playground with a self-checking testbench covering overflow, underflow, reset behavior, and simultaneous read and write pointer logic to ensure functional correctness.

GitHub: github.com/stavanrupareliya36/fifo-design-verification

UART Transmitter & Receiver | **RTL Design** *Verilog; EDA Playground*

- Designed a UART transmitter and receiver in Verilog RTL with configurable baud rate, implementing FSM-based control for start/stop bit framing, serial-to-parallel data conversion, and parity generation/checking for reliable serial communication.
- The simulated design was validated on EDA Playground using directed testcases and loopback testing, verifying data integrity across multiple baud rates and error conditions such as framing and parity errors.

GitHub: github.com/stavanrupareliya36/uart-design-verification

Binary Artificial Neural Network | **ASIC Design** *Verilog; ModelSim, Synopsys*

- Designed an RTL logic single-layer Binary Convolutional Neural Network which constituted a max-pooling layer on a randomized input matrix and kernel matrix extracted from 2 SRAMs using Verilog.
- The simulated design was validated using ModelSim. Synthesis was performed by using Synopsys Design Compiler to achieve minimum area and maximum throughput.

GitHub: github.com/stavanrupareliya36/binary-neural-network-asic

Certifications

- **Digital Design – Hands-on** *Maven Silicon*
  Hands-on training in digital logic: combinational & sequential circuits, FSMs, and memories.
- **Verilog HDL – Hands-on** *Maven Silicon*
  Practical RTL design using Verilog: combinational & sequential logic, FSMs, and simulation.
- **VLSI System On Chip Design – Overview** *Maven Silicon*
  Overview of SoC design flow: architecture, IP integration, RTL design, and verification.
- **Verification Methodology Overview** *Maven Silicon*
  Fundamentals of verification: SystemVerilog, UVM concepts, testbench architecture, and coverage.

Invited Talks & Guest Lectures

Nirma University, Institute of Technology | Expert Speaker for B.Tech Students Jan 2024

- Delivered an Industry Expert Lecture on **Embedded AI & Computer Vision Applications** at **Nirma University, Institute of Technology,** covering real-time AI deployment, embedded optimization, and edge intelligence.

Nirma University, Institute of Technology | Expert Speaker for M.Tech Students Aug 2024

- Delivered an Industry Expert Lecture on **Edge Computing and Computer Vision** for **M.Tech students specializing in VLSI and Embedded Systems.**

eInfochips (An Arrow Company) | Nirma University STTP Sep 2024

- Represented eInfochips (An Arrow Company) as an Expert Lecturer at the Faculty Development Program (FDP), Institute of Technology, Nirma University, Ahmedabad, delivering a session on **"Edge Computing and Computer Vision"** focused on NVIDIA Edge AI.

Indore Institute of Science and Technology (IIST), Indore | Adratim Adhiratham 2.0 Jun 2026

- Invited to deliver an expert talk on **"Edge AI"**, covering AI hardware accelerators, computer vision, deployment pipelines, model optimization, and real-world Edge AI applications.

Nirma University, Institute of Technology | STTP on Edge AI and Vision Jul 2026

- Delivered an invited expert talk on **"Edge AI and Vision"** under the STTP program, presenting **"Deep Dive into Edge AI: Concepts to Deployment"** to researchers and faculty members.

Technical Publication

Journal Paper 2020	The visual computer, An International Journal of Computer Graphics, Springer Publication, 2020 “Real-time detection and identification of plant leaf diseases using convolutional neural networks on an embedded platform", Springer Publication. Paper Link
Conference Paper 2021	2nd International Conference on Communication, Computing and Industry 4.0 (C2I4) , 2021. “Real-time Face Mask Detection System on Edge using Deep Learning and Hardware Accelerators”, IEEE Publication. Paper Link
Conference Paper 2021	Proceedings of the International e-Conference on Intelligent Systems and Signal Processing, 2021. “Real-Time Tomato Detection, Classification, and Counting System Using Deep Learning and Embedded Systems”, Springer Publication. Paper Link
Conference Paper 2022	Advances in VLSI, Communication, and Signal Processing, 2022 “Face Mask Detection and Counting Using Deep Learning and Embedded Systems", Springer Publication. Paper Link

Awards & Recognitions

Core Value Award - Customer First 2024

- Recognized for exceptional dedication to prioritizing customer needs, resulting in increased customer satisfaction and loyalty. Demonstrated an outstanding ability to address customer concerns and ensure a positive customer experience.

Pat On The Back Award 2022

- Honored for exemplary performance and significant contributions to an image processing project. Demonstrated exceptional leadership, teamwork, and problem-solving skills, consistently exceeding expectations.

Education

Master of Technology (M.Tech), Embedded Systems Engineering Jun 2018 – Jun 2020
Institute of Technology, Nirma University, Ahmadabad, India.

Bachelor of Engineering (B.E), Instrumentation and Control Engineering Jun 2012 – Jun 2016
Atmiya Institute of Technology, Gujarat Technological University (GTU), Rajkot, India.